TELEVISION RECORDING OPERATIONS

Handout Number: 5

AVR-2 TIMEBASE CORRECTOR

- A detailed look

Written by : Jeremy Brown

Issue : One

Date : March 1981

INTRODUCTION

This handout will concern itself with an investigation of an AVR-2 Digital Timebase Corrector (DTBC) and will do so in two parts. Firstly the principles of operation will briefly be sketched and this will be followed by a general functional look at the D.T.B.C. board by board, paying particular attention to the Random Access Memory and the method of Horizontal Timing used. However, before we go any further, let us consider a few points about digital timebase correction. The reader is assumed to understand the basic needs and methods of analogue correction.

1.1. Digital Timebase Correction

Timebase correction is used to correct the replayed signal, so that any mechanical instabilities in the record/replay process are minimised and so that the replayed signal can be made synchronous with a known reference signal. The main advantage in using digital techniques for this process, as opposed to analogue, is that apart from quantizing errors, inherent in the A-D and D-A process, no other losses in quality are suffered and hence, the delay-line can be as long as we like without suffering from added picture degradation. This means that the specification of the servo systems of the AVR-2 need not be as tight as they were on previous machines.

1.2 The Input Signal Requirements of a D.T.B.C.

(a) The correction can shift the timing of an off-tape line by up to $\pm\frac{1}{2}$ a line and therefore, the demodulated video must be replayed to the reference within that range.

(b) The signal is assumed to be colour; however if a monochrome signal comes off the tape a pseudo burst, derived from off-tape line syncs, is added prior to timebase correction and it is then treated as a colour signal. The burst is removed at the output.

(c) Since the timebase corrector does not transcode or decode the signal, both the recorded and reference signals must conform to the PAL standards, particularly in relation to the colour-subcarrier and sync frequency.

2.1 An Outline of the General Operation of the Corrector

As has already been stated, the unit can cope with errors of up to $\pm\frac{1}{2}$ a line either side of a suitable reference signal. The input to the corrector is off-tape demodulated video, which is phased $2\frac{1}{2}$ lines early with respect to station syncs. This signal is then clamped, corrected and finally sent out as a stabalized output, re-timing having been carried out on a line to line basis.

Correction is carried out in the following sequence:

(i) Each line is sampled at three times tape subcarrier frequency. (13.3 MHz). This choice of sampling rate reduces beat patterns and it is derived directly from the burst on the back porch of the sampled line.

(ii) Each sample is converted into an 8 bit digital word which represents the voltage level of each sample. With a maximum of 256 levels each step would be about 5mV on a standard video signal.

(iii) Three 8 bit words are sequenced and converted into a 24 bit word which is then fed into a Random Access Memory. A 24 bit word was chosen since it could be handled more slowly than three 8 bit ones, as only "slow" R.A.M.s were available at the time of design.

(iv) Data words are read out of the memories at a rate synchronous with a suitable reference. Since the data was written into the memories at a rate containing the timebase error, but read out of them at a stable reference rate, timebase correction has occured. The correction is carried out in two stages:

(a) Vernier - Correction:- The vernier correction is that fraction of a subcarrier cycle which represents the phase difference between off-type subcarrier and the stable reference subcarrier. In vernier correction, the timebase error is corrected to the nearest whole increment of a reference subcarrier period, thus removing any phase error between the off-tape subcarrier and the reference. Any residual error is then corrected by the coarse timebase corrector.

(b) Coarse-Correction:- The Coarse correction is that number of whole subcarrier cycles which represents the time difference between off-tape and reference sync pulses. The coarse corrector corrects errors from plus or minus one period of subcarrier to plus or minus half a line period.

(v) Any required dropout and velocity compensations are now made. Velocity compensation is nearly always needed because the timing of an off-tape video signal may change during the sweep of a head. These changes may be brought about by a difference between record and replay guide height, tip penetration and guide radius. Now, since the timebase corrector only correctly times the beginning of each line, any changes in timing during that line will show up as a phase difference across the picture; hence the need for velocity compensation.

(vi) The corrected data words are sent to a Digital to Analogue converter and appear as the machine output.

Correction has now been achieved. Let us examine the system in a little more detail, stage by stage. Reference should now be made to the diagram on the following page.

3. THE OPERATION OF THE DIGITAL TIMEBASE CORRECTOR

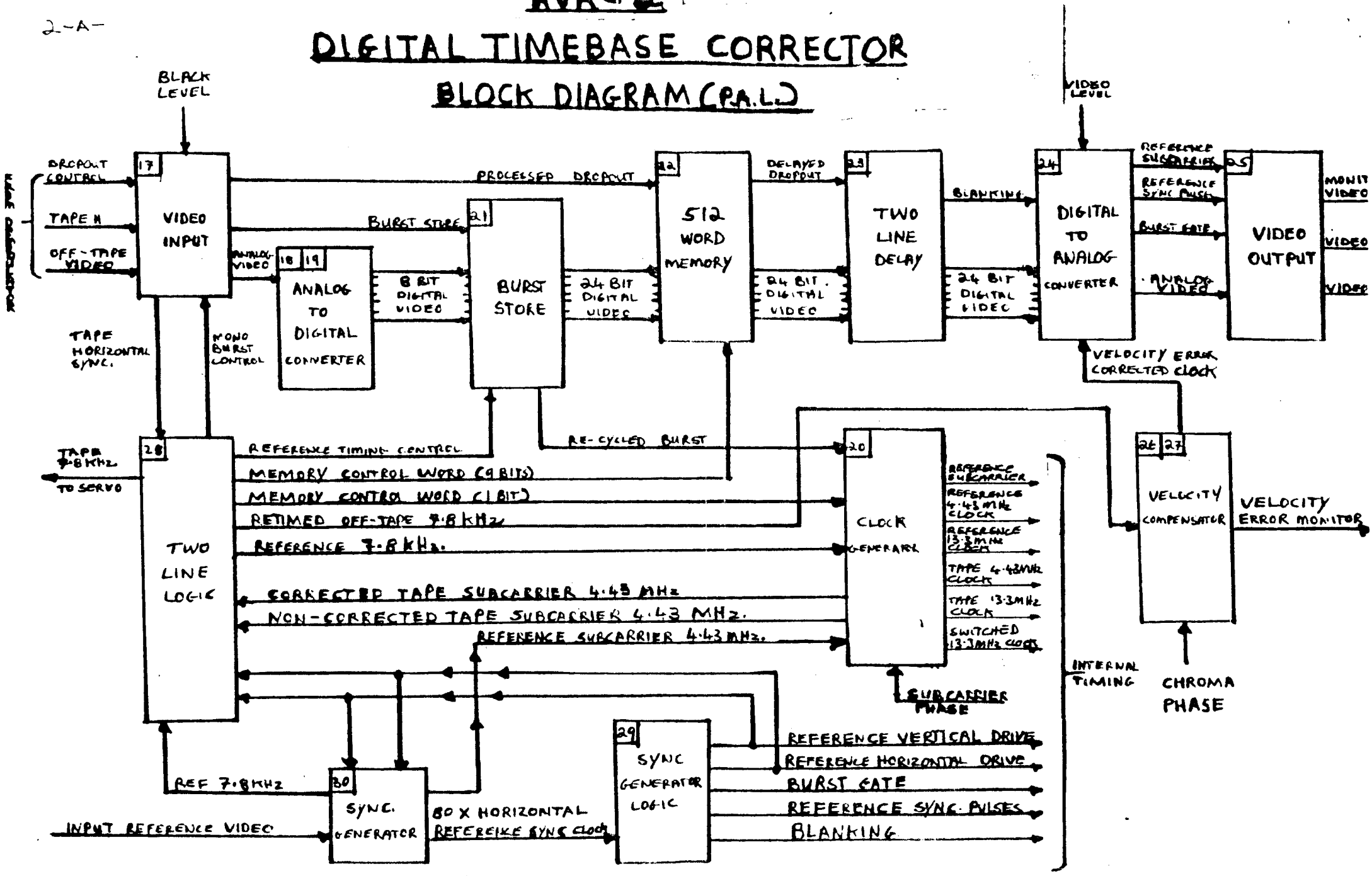
3.1. Video Input (Board 17)

(a) The demodulated, off-tape video is clamped and sent to a video insert switch, to provide a D.C. reference level for Analogue to Digital conversion.

AVR-2

DIGITAL TIMEBASE CORRECTOR

BLOCK DIAGRAM (PAL)



J.M.A

Video Input (Board 17) Contd....

(b) Should the input signal be monochrome, a burst is generated on board 28 and is inserted onto the video in the usual place. The burst is removed after processing before output. A ringing oscillator, triggered by horizontal line timing, is the method of regenerating burst and this synthesized signal contains the timing errors of the off-tape signal.

(c) The output of the video insert switch is amplified, with adjustable black-level, and low pass filtered before it is sent to the next set of boards for Analogue to Digital conversion. This board also tells the "Burst Store" when to store information relating to the burst and also senses whether or not a dropout is present: A dropout being a -20dB loss in relative F.M. signal level.

The Analogue to Digital Converter (Boards 18 and 19)

3.2. Analogue to Digital conversion is carried out in two stages, called A and B. Stage A produces the four most significant bits, whilst B produces the four least significant bits. A two stage method of conversion is used because it is relatively quick, cheap and only 32 reference levels plus an accurate subtractor are required.

Stage A receives video at samples of 3 times tape burst subcarrier frequency (Fcsct). (Or 3 times synthesised Fcsct., in the case of monochrome). This sample is then sent to a D - A converter and a delay-line, equal in length to the time the D - A will take to convert the signal. A 4 most significant bit word is produced and this is sent, with the delayed analogue signal, to stage B.

Both channels of information arrive at B and the digital information from A is temporarily stored until B has produced the 4 least significant bits. Meanwhile the digital signal from A is sampled and converted back to an analogue signal, this is then subtracted from the delayed analogue signal that left A and the remainder is converted into a digital signal. The 4 least significant bits have now been produced by stage B. The digital output from A and B are now serially combined to produce an 8 bit word representing the sampled video input. This word is next sent to the "Burst Store".

Burst Store (Board 21)

3.3. This stage is concerned with vernier timebase correction and the conversion of three 8 bit words into a single 24 bit word, for subsequent rapid handling. It also produces a frequency, for a whole line period, equal in frequency and phase to that of the off-tape burst, for that line.

Three consecutive 8 bit words are put into eight 3 bit serial to parallel converters, thus producing a 24 bit word. Each 8 bit word arrived at 3 x F csct but each 24 bit word is only completed at F csct $\frac{1}{3}$ of the arrival rate. For the remainder of it's journey through the processor, the signal will be handled at F csct rate. Data from the serial to parallel converter is next fed into a 2 x 24 bit Random Access Memories (RAMs). The vernier correction, that is the retiming of the off-tape signal to match the nearest frequency of reference subcarrier (Fcscr), is performed in this RAM as follows:

Burst Store (Board 21) Contd...

Correction is made by simply writing each word into the RAM at Fcsct rate, but only reading it out at Fcsc rate. A control signal from the "Logic Control Board" (see later), representing the approximate phase relationship between the two signals, determines whether the word is read from the first or second memory file. The vernier corrected signal is next sent to a 512 word RAM.

The Burst Store's other function is to produce a frequency equal to that of the burst for a whole line period. Information, telling the store when a burst is due to arrive is sent from the input board. A 16 x 8 RAM then stores the burst information in 15 words and continually re-circulates the information for the rest of the line. This information is then sent to a D - A converter and the Burst Store emits subcarrier in phase with off-tape burst for the remainder of the line. This new signal is sent to the clock generator.

512 Word Memory (Board 22) (For the choice of delay time ; see appen. one)

3.4. This section is concerned with applying coarse timebase correction to the vernier corrected signal. First the 24 bit word from the Burst Store, is combined with a 1 bit dropout information word concerned with those three samples, previously derived on the input board, and a 25 bit word is formed. The new word is filed in an array of 512 x 25 bit RAMs and by processing the 24 bit video word with the dropout information, coarse timebase correction is applied to both simultaneously. Coarse correction is achieved by relating a memory read address which is equal to the correct write address, plus a count which is equal to the coarse TBC, in whole multiples of subcarrier frequency.

The write address is incremented sequentially by a reference subcarrier. clock whilst the read address is generated by subtracting a memory control address from the write address. The memory control is generated on the logic board and represents the amount of correction needed (see later). Since vernier correction has been carried out, the logic board need only provide a correction signal in discrete cycles of subcarrier. The signal has now been fully corrected, with respect to time, and represents a full colour signal.

The 512 Word RAM

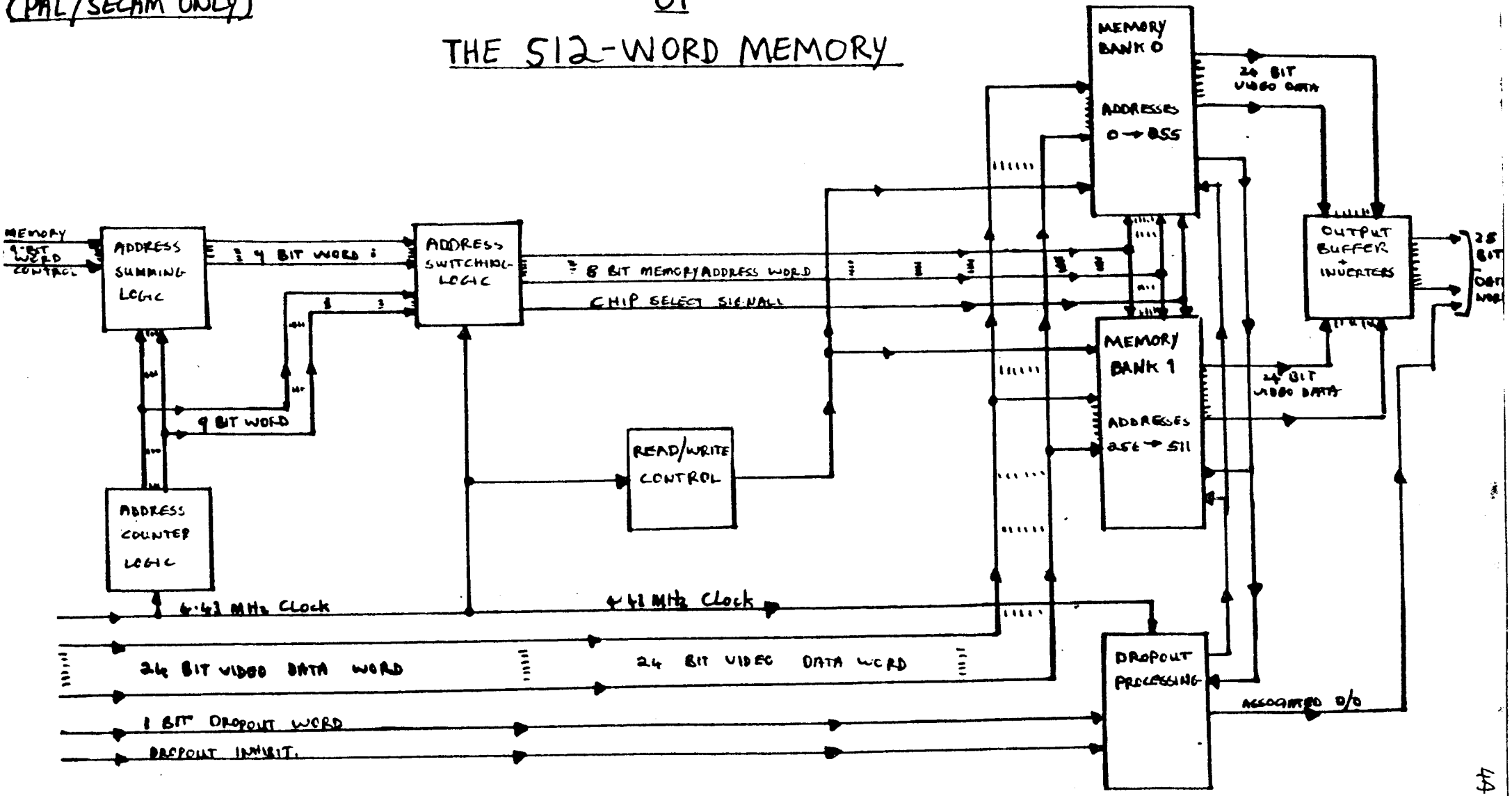
3.4A Let us now examine the arrangements of the RAM in a little more detail. The random access memory provides rapid access storage for just under 2 horizontal lines of digital video information. Each line is represented by 284 25 bit words (the number of cycles of subcarrier per line).

The RAM consists of fifty, 256 x 1 bit IC memories; that is a 512 x 25 bit word capacity. Each IC provides one output for the data and contains eight address inputs, one chip select input, a write enable input and a data output. The ICs are arranged to provide 2 banks of memories; memory bank 0 caters for words 0 - 255 and memory bank 1 for words 256 - 511.

BOARD 22

(PAL/SECAM ONLY)

A DIAGRAM OF THE BLOCK FUNCTION OF THE 512-WORD MEMORY



3/81 JMB

The 512 Word RAM (Contd...)

The eight address lines on each of the 50 ICs are all tied together in parallel; that is all the address word 1 wires are paralleled as are 2 and 3 etc. Now, when the address logic sends out an address, the same location in each of the 50 chips will be accessed and that location may be from 1 to 255. But, as has already been mentioned, although there are 50 chips available, only 25 are needed per word. So, the final discrimination, as to which bank of 25 should be selected, is carried out by the "chip select" signals. These signals are so arranged that only one bank of 25 can be selected at a time. Thus, although the address only appears to be an 8 bit code, the chip select does, in fact, make it a nine bit code with access to 512 locations.

In short, in order for a word to be written into a specific location, the 8 address lines must contain the 8 bit address of the memory location, the chip select to that bank must be low and the write enable to that bank must be low. The write enable signal is tied in parallel to all the chips in both banks, the contents of the 25 data lines being written into those chips that have a low chip select.

In order to read a memory the process is very similar to that of writing. The appropriate 8 bit address is required, chip select must be low and write must be high. So, as we can see, read and write are the same, except write enable must be low to write and high to read. During recording and writing all the data outputs/inputs from each bank are arranged in parallel, so as to form 25 bit words. Since static RAMs are used, no refreshing signals are needed.

The Dropout Compensator (Board 23)

3.5 This assembly is used to provide dropout compensation and the delay required for velocity error calculation. A 24 bit word of video, with it's associated dropout bit, arrives from the RAM and is fed into a series of shift registers which provide a 2 line delay. Each delay register, for each bit, consists of two 256 bit registers connected serially; therefore, 25 pairs of these are needed for the 25 bit words. These words are moved through at reference subcarrier frequency taking only 512 steps to provide a 2 line delay, since the information is not moved during line blanking.

So, in order for dropout compensation to work, each 25 bit word is clocked through the 2 line delay and, if a dropout bit arrives at the output, the input is immediately corrected to the output, thus substituting the faulty video with video from 2 lines later. The missing video has thus been replaced.

The Digital to Analogue Converter (Board 24)

3.6 This takes the output from board 23 and converts it from digital to analogue form. The rate of conversion is used to provide velocity compensation. The rate at which conversion should take place is controlled by the velocity compensator board, which can also be used to adjust the chroma phase. The corrected analogue video is fed to the output stage in discrete steps.

3.7 Video Output (Board 25)

This circuit provides gain control, filtering, level shifting and clamping of the re-sampled video. Syncs and burst are re-inserted using the syncs and burst from the reference video. The output is now fully corrected and suitable for studio use. However, at this point, we should note that, unlike the VR 2000 machines, the VPR 2 machine outputs are not sure-sync.

3.8 Boards 20,29 and 30

These boards provide the reference timing signals used by the timebase corrector and their accuracy depends on the accuracy of the input reference fed to them. The basic D.T.B.C. has its own internal oscillator and it can, therefore, act independently of external references.

However, when in normal studio use, the external reference genlocks onto the appropriate incoming reference. Normally it would genlock onto incoming video when in an E to E mode, record mode or edit mode and it would genlock onto reference video, for example black and burst, when in a reply mode.

We should note that when the D.T.B.C. is referred to an input video a 15 us phase advance is inserted by the sync generator, so that the video output will not be timed to station reference.

3.8A The Sync Generator (Board 30)

This board is used to generate a crystal controlled reference sub-carrier and, when an external reference is used, the crystal is phase locked to that reference.

When a burst is not present the oscillator is phased to a $\frac{1}{4}$ reference H rate signal derived from board 29: Board 30 also provides a 7.8 KHz. V.A.S. signal and an 80 x ref, H clock frequency.

3.8B The Sync Generator Logic (Board 29)

Uses the 80 x reference H clock frequency to derive the majority of timing signals used by the D.T.B.C. the outputs are shown on page 5.

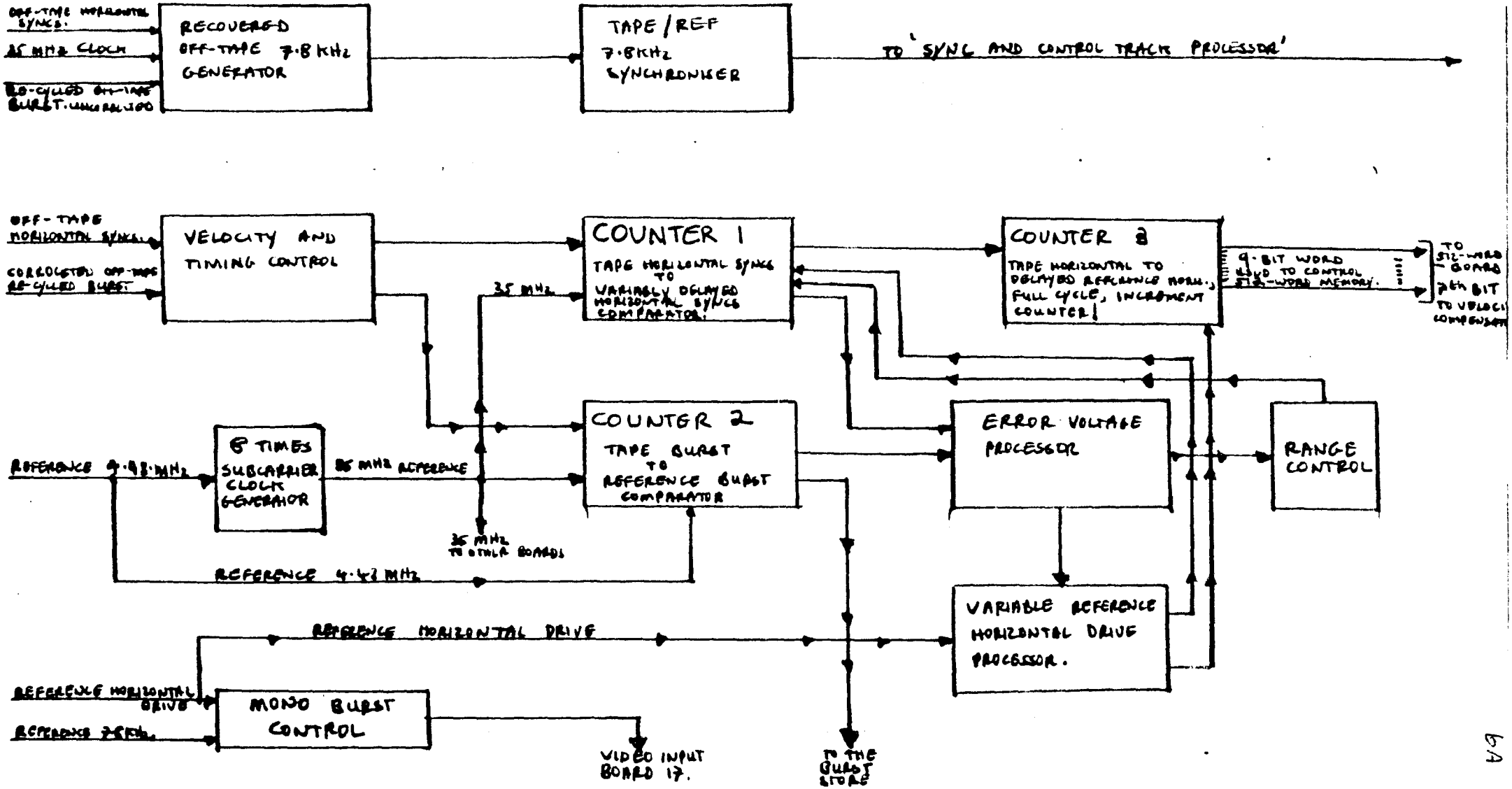
3.8C Clock Generator (Board 20)

Provides most of the clocking frequencies used by the D.T.B.C. the outputs of which are shown on page 5. Provision is also included to unblank selected lines during the vertical interval so as to gate VIT signals through the video board.

3.9 Two Line Logic (Board 28)

This circuit is mainly concerned with making two measurements. The first one it makes is the time difference between off-tape line syncs and reference line syncs. This coarse correction, as the error has been called, is expressed in terms of a 9 bit word, which is fed to the 512 word RAM, and controls the clock out rate from that device. Meanwhile, the 7th bit, of the error word, is fed to the velocity compensator (see later) and informs it whether the error is greater than, or less than, half a line.

A SIMPLIFIED BLOCK DIAGRAM OF LOGIC BOARD 28



6A

3/81 DMO

Two Line Logic (Board 28) Contd...

The nominal value of the centre word, that is with no error, is 141 cycles of sub-carrier: The head servo being advanced by about 2½ lines with respect to reference syncs.

The other main role of the circuit is to provide the "Burst Store" with information about the vernier correction needed. This vernier error is derived from the time difference between a positive going transition of reference subcarrier compared with a positive going transition of off-tape subcarrier.

The two line logic board has to carry out two more functions. It has to provide a correlation between an error derived from the off-tape burst and that from off-tape sync; this is done to avoid errors of up to a cycle of subcarrier being introduced by the memory control. Finally, an off-tape 7.8 KHz signal, derived from an examination of the sync/burst timing relationship, is also generated.

3.9 (i) The Operation of the Two-Line Logic Board

Let us examine this board in a little more detail: A simplified block diagram of its layout is shown overleaf.

The input signals to the board are shown in the diagram. The only extra signal needed is a 35 MH, clock signal, which is used by the board for timing purposes. This clocking signal is derived on the board itself from reference subcarrier.

3.9 (ii) Let us look at the methods of timing error detection used. The "Delay and Timing Control" receives regenerated, off-tape, burst frequency, with V.A.S. removed. This device also received a feed of off-tape horizontal sync pulses. Now, before any timings are made, we have to make sure that the off-tape burst received corresponds to the correct horizontal line. This is obviously essential when comparing the outputs of counter No. 1 with counter No. 2, as we shall see later. Since we cannot receive any new information about the burst relating to a leading edge of line sync until the burst of that line has passed through the system, there will be a lag of at least line sync duration (4.7 us) plus the breezeway duration (0.8 us), that is at least 5.5 us, until the burst arrives. Therefore, in order to make sure we have the correct burst, the off-tape horizontal signal is delayed by an arbitary value of 8.6 us, in order for the burst to "Catch-Up".

After this delay, the device sends an off-tape horizontal sync rate signal, clocked at tape subcarrier frequency to counter No. 2, so that a verner correction signal can be derived. Also, it sends the same horizontal signal to counter No. 1, so that the coarse correction signals may be calculated.

3.9(iii) Counter No 2 measures the difference between the leading edge of a cycle of re-circulated burst, fed from the "Delay and Timing Control", and the leading edge of reference burst. The difference is expressed in eights of a cycle of subcarrier, from the 35 MHz clock signal: An accuracy to only an eighth of a cycle of subcarrier is needed because the logic board has only to establish whether the error is greater, or less than half a line from the "Burst Store" and whether the error is greater or less than one cycle for the 512 word RAM. We should note, at this point, that the "Burst Store" is responsible for the accurate vernier timing of the signals and only uses the logic board to help it, whilst the 512 word RAM only needs signals accurate to the nearest cycle of subcarrier in order for it to function correctly.

We have said that counter No. 2 measures the difference, to the nearest eighth of subcarrier period, between off-tape burst and reference burst. Now, this number can be anywhere between 0 and 7, the counter having been reset each time it reached 8. This value is sent to the "Error Voltage Processor" for later comparison with a similar line-timing counting counter 1. It's value is also sent to the "Variable Horizontal Drive Processor" for later feed back correction of the timing detection errors. Finally, an output is used to tell the "Burst Store" if the difference between tape burst and reference burst is greater or less than half a cycle. If it is greater than half a cycle, counts 4 to 7, a logic 1 is sent to the store at its output is read from a whole and partial memory delay; if it is less than half a line, counts 0 to 3, a logic zero is sent to the store and its output is read from partial memory delay. The "Burst Store" is left to carry out detailed vernier correction, whilst the logic board determines the coarse timing error.

3.9(iv) Counter No. 1 measures the time difference between the arrival of the delayed horizontal tape line signal and the arrival of the variable delayed, reference horizontal signal, which we shall come to later. The difference in time is expressed, as in counter No. 2, to the nearest eight of a cycle of subcarrier. Now, because of the servo-phasing being in advance of the reference signal, about half a horizontal line period (32 us) of cycles are normally counted (141). Each time the counter reaches 8 it is reset and a carry signal is sent to counter No. 3. So, when counter No. 1 stops at the end of the timing period, it will have sent out two pieces of information. Firstly, the number of whole cycles of reference subcarrier passed, that is the coarse timing error, and the number of eights left as a remainder, that is another measure of vernier error. This vernier error, like that from counter No. 2, is fed to the "Error Voltage Processor" for comparison.

3.9(v) Now, let us examine the "Error Voltage Processor". Basically, this looks at the outputs of counters 1 and 2, to see if they are the same. If they are not, this means that there is an error in the calculation of timebase errors between the off-tape burst signal (via counter 2) and the off-tape horizontal signal (via counter 1). Hence, an error of up to ± 1 cycle of subcarrier may be sent to the memory control. To overcome this, and to make both error counters read the same, feedback is applied to counter No. 1 to make its count equal to that of the burst error from counter No. 2, Thus the burst error has priority over the line error.

The output of the "Error Voltage Processor" is fed to two correction sources. Firstly, the "Range Control", which provides major correction facilities and secondly, to the "Variable Horizontal Drive Processor", which provides minor correction facilities.

3.9 (vi) If, on arrival at the Range Control, the error voltage is outside prescribed limits the device sends a coarse correction signal back to counter No. 1 to bring its output in to line with counter No. 2.

3.9(vii) Meanwhile, the "Variable Horizontal Drive Processor" has received an error signal, as well as a feed of reference horizontal drive, derived from the reference source. If there is an error, it looks at both of these signals and works out the time at which the reference H drive signal was detected. It then sends a suitably delayed horizontal drive signal to counter No. 1, so that it produces the same 0-7 count as counter No. 2. Now, errors of up to $\pm$ 1 cycle of subcarrier cannot be sent to the memory control.

We have seen how a vernier correction is measured in two ways, that is from burst to burst and sync to sync, and we have seen how the two are made to agree. We have also noted that the "Burst Store" actually carried out the vernier correction whilst the logic board only provided information as to which set of memories should be read out.

All we have to do now is to provide the information required by the 512 Word Memory Control, to tell it by how many cycles of subcarrier it should delay its readout. The information is in the form of a 9 bit word and is formed in counter No. 3.

3.9(viii) Counter No. 3 receives, from counter No. 1, the time difference in whole cycles of subcarrier between processed horizontal reference syncs and tape reference syncs, as well as a feed of the "Variable Horizontal Drive Processor". Basically, it converts the whole number of cycles to a 9 bit word and sends it to the memory control of the 512 word RAMs, at processed horizontal drive rate. At the same time, the 2 7th bit is fed to the velocity compensator which tells it whether the error is less than or greater then half a line.

We have seen how timing errors are calculated on board 28 and the only other functions left for it to do are the generation of a pseudo burst from monochrome horizontal demodulated signal and the field phasing of tape replay, via the control track. Both these functions are shown in the diagram.

3.10 <u>The Velocity Compensator</u> (Board 26)

This circuit compares the phase difference between the burst signals at the beginning of successive lines and determines the magnitude of the velocity error. This error is converted to a D.C. signal which powers a linear ramp generator whose output amplitude is proportional to the phase error. The magnitude of the ramp is converted back to a digital signal and this controls the rate at which the main D-A converter is clocked. The output clocking rate is thus used to control the velocity errors which show up as horrible phase changes on coloured pictures.

The chroma phase of off-tape pictures can also be adjusted by varying the amplitude of the ramp. Thus, the ramp amplitude is "tweaked" to provide a phase control!

4.0 Conclusion

We have now come to the end of our journey through the AVR-2 digital timebase corrector. We have seen how, by the use of digital techniques, the stabilization of demodulated video can be achieved and we have seen how large words have had to be made up to cope with the slow clocking rites of early RAMs. However, despite its apparent complexity, the AVR D.T.B.C. is a very reliable beast and is forerunner of the modern VPR2 timebase corrector.

Appendix 1 : How big should the memory be?

If we were to examine an N.T.S.C. AVR-2 D.T.B.C. memory, we would find that it could provide ± half a line of storage and would need 256 words. However, we have seen that the 625 PAL system needs 512 words, why should this be?

The answer is quite simple. Both systems need one line of storage, and the number of words needed is equal to the number of cycles of subcarrier in a line.

We cannot economise, as we did in the 2-line delay, since when the words go into the memory we do not know where line blank or field blanking is.

Therefore the number of cycles of subcarrier in 1 line N.T.S.C. =

$$\frac{3.58\ \text{MHz}}{30 \times 525} = 228 \text{ words}$$

i.e. the nearest binary RAM = 2 = 256 words. The mid operating point would be about 114 words.

In PAL-D, no. of cycles = $\frac{4.43\ \text{MHz}}{25 \times 625}$ = 284 words.

i.e. the nearest binary RAM = 2 x 2 = 512 words. The mid operating point, would be about 141 words, therefore a considerable part of the memory is not used!

References

AVR-2 Theory of operation, Ampex.
AVR-2 Points and Schematics, Ampex.

J. Brown : 30.01.81